Claims

What is claimed:

1. A system for automatically generating and validating a memory test model for an electronic device, the system comprising

a memory test model generator for inputting memory characteristics for the electronic device and for outputting a memory primitive; and

a memory test model validator for validating the memory primitive for generating a memory test model for the electronic device.

2. The system of claim 1, wherein the memory test model generator includes a graphical user interface for inputting the memory characteristics.

3. The system of claim 1, wherein the memory test model generator includes a memory model maker for selecting a template for the memory primitive and for utilizing the memory characteristics to customize the memory primitive.

4. The system of claim 3, wherein the memory model maker translates port arbitration information for the electronic device into a test framework language before adding the port arbitration information to the memory test model.

5. The system of claim 1, wherein the memory characteristics are input using memory description language.

6. The system of claim 5, wherein a portion of the memory characteristics are written in a memory description file using the Memory Description Language, said file associating particular memory characteristics with particular memory primitives.

7. The system of claim 1, wherein the memory primitive represents an irreducible memory structure that is suitable for at least one of a register transfer-level simulation, a timing analysis, a test generation and a fault simulation.

8. The system of claim 7, wherein the memory primitive includes at least one of a random access memory primitive, a content addressable memory primitive, and a first-in-first-out memory primitive.

9. The system of claim 8, wherein the random access memory primitive is a single port memory primitive having an address decoder, an enable pin, and a bi-directional pin for writing and reading data.

10. The system of claim 8, wherein the random access memory primitive is a dual port memory primitive having two address decoders, read and write enable signals, an output enable pin, a read data pin, and a write data pin.

11. The system of claim 8, wherein the content addressable memory primitive has at least one read port, values on a compare data port being compared with a corresponding read port with the result compressed into one bit.

12. The system of claim 8, wherein the first-in-first-out memory primitive has read and write addresses that are handled internally.

13. The system of claim 1, wherein the memory test model validator processes a gate-level description to produce test patterns and report fault coverage.

14. In an electronic device, a method for automatically generating and validating a memory test model, the method comprising the steps of:

inputting memory characteristics for the electronic device;

processing said memory characteristics to produce a memory primitive;

validating said memory primitive; and

generating a memory test model for the electronic device from the validated memory primitive.

15. The method of claim 14, further comprising the step of:

after the step of inputting, creating a memory description file to store a portion of the memory characteristics, said file written in memory description language.

16. The method of claim 14, wherein, in the step of processing, the memory primitive includes at least one of a random access memory primitive, a content addressable memory primitive, and a first-in-first-out memory primitive.

17. The method of claim 16, wherein, in the step of processing, the memory description file is utilized to form a memory primitive template for producing the memory primitive.

18. The method of claim 14, further comprising the step of selecting a template for the memory primitive and for utilizing the memory characteristics to customize the memory primitive.

19. The method of claim 14, wherein the step of processing includes the step of processing a gate-level description to produce test patterns and report fault coverage.

20. The method of claim 19, wherein the step of processing further includes the step of matching a first response of the test model associated with the test patterns to a second response of a register transfer-level model associated with the test patterns, a close match indicative of the equivalence of the test model and the register transfer-level model to validate the memory primitive.

21. A computer-readable medium that stores a program for automatically generating and validating a memory test model for an electronic device, the program comprising

a memory test model generator for inputting memory characteristics for the electronic device and for outputting a memory primitive; and

a memory test model validator for validating the memory primitive for generating a memory test model for the electronic device.

22. The computer-readable medium of claim 21, wherein the memory test model generator includes a memory model maker for selecting a template for the memory primitive and for utilizing the memory characteristics to customize the memory primitive.

23. The computer-readable medium of claim 21, wherein the memory model maker translates port arbitration information for the electronic device into a test framework language before adding the port arbitration information to the memory test model.

24. The computer-readable medium of claim 21, wherein the memory primitive represents an irreducible memory structure that is suitable for at least one of a register transfer-level simulation, a timing analysis, a test generation and a fault simulation.

25. The computer-readable medium of claim 24, wherein the memory primitive includes at least one of a random access memory primitive, a content addressable memory primitive, and a first-in-first-out memory primitive.

26. The system of claim 25, wherein the random access memory primitive is a single port memory primitive having an address decoder, an enable pin, and a bi-directional pin for writing and reading data.

27. The computer-readable medium of claim 25, wherein the random access memory primitive is a dual port memory primitive having two address decoders, read and write enable signals, an output enable pin, a read data pin, and a write data pin.

28. The computer-readable medium of claim 25, wherein the content addressable memory primitive has at least one read port, values on a compare data port being compared with a corresponding read port with the result compressed into one bit.